

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE
(UGC-AUTONOMOUS INSTITUTION)

Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi
NAAC Accredited with A+ Grade, NIRF India Rankings 2022 - Band: 251-300 (Engg.)
NBA Accredited - B.Tech. (CIVIL, CSE, CST, ECE, EEE, MECH), MBA & MCA
www.mits.ac.in

EXAM SECTION - NOTIFICATION DATE: 30.01.2025

M. Tech I Year I Semester II Mid – Term Test Schedule February – 2025

Academic Year – 2024 – 25

Timings: FN: 09:30 AM to 11:30 AM
AN : 03.00 PM to 05.00 PM

| DATE / DAY/SESSION | | VLSI & EMBEDDED Systems |
|--------------------------|----|---------------------------------------------------------------------------|
| 24.02.2025 (Monday) | FN | CMOS Digital IC Design- 24VESP101 |
| | AN | Microcontrollers and Programmable Digital Signal Processors- 24VESP102 |
| 25.02.2025 (Tuesday) | FN | FPGA Architectures and Applications-24VESP403 |
| | AN | Low Power VLSI Design-24VESP404 |
| 27.02.2025 (Thursday) | FN | Research Methodology and IPR-24RMP101 |
| | AN | Disaster Management-24AUP901 |

Note: 1. HOD is requested to circulate among the faculty in the department.



Controller of Examinations

CONTROLLER OF EXAMINATIONS

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

Copy to:

1. HOD Madin Road Angali
2. HOD Madanapalle 517 425-01
3. Copy to HOD to be read in M. Tech , I Year I Semester Class Room
4. Notice Board (AS & Dept)
5. File (AS)



PRINCIPAL

Principal

**Madanapalle Institute of
Technology & Science
MADANAPALLE**

E Copy To: Vice Principal (Academics)-UG Vice Principal (Academics)-UG Vice Principal

(Administration) HOD SAO (G) PRO SWO SAO(Systems) Dy. Warden

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